SPECIFICATION

Please replace paragraph [0036] with the following new entry:

[0036]   FIG. 10 shows a fourth embodiment of phase shifter **413**. It comprises a voltage-controlled oscillator **1001**, variable delay circuits **1003, 1004, 1005**, and a dummy buffer ~~1002~~**1002**. It does not need the input clock **402** because it uses a voltage-controlled oscillator as a clock source. A voltage-controlled oscillator is controlled by `PC1` **411** and generates a clock whose frequency is adjusted so that the phase of `CLK2` **415** is located at the optimum sampling position. Variable delay circuits **1003, 1004, 1005** are controlled by `PC2` **412** and generates `CLK1` **414**, `CLK2` **415**, and `CLK3` **416**, respectively. The dummy buffer **1002** is an optional circuit that could be included so as to match the phase difference between the three clocks **414, 415, 416** equally. For the embodiment of FIG. 10, the phase of `CLK2` **415** should be controlled by `PC1` **411** only and should not be affected by the variation of `PC2` **412**. And the phase differences between the three clocks **414, 415, 416** should be affected by `PC2` 412 and should not be affected by the variation of `PC1` **411**. If frequency range of the voltage controlled oscillator **1001** is wide, it may be difficult for the phase of `CLK2` **415** to track the optimum sampling position because of the initial acquisition failure. To avoid this difficulty, we can add a reference loop. See Richard Gu et al, "A 0.5-3.5 Gb/s Low-Power Low-Jitter Serial Data CMOS Transceiver," ISSCC Digest of Technical Papers, pp.352-353, February 1999. Upon power-up or reset, the data recovery system is defaulted to the reference loop so that the frequency of the voltage controlled oscillator **1001** output is locked to an external reference clock. After initial lock is acquired, the loop containing the signals `PC1` **411** and `PC2` **412** is enabled.

Please replace the as-filed abstract with the new abstract on the next page: